## Remarks/Arguments

The Office Action mailed on May 29, 2009 has been reviewed and carefully considered. Claims 1, 7 and 12 have been amended. Claims 1-17 are currently pending in this application. No new matter has been added. Reconsideration of the above-identified application in view of the following remarks is respectfully requested.

Claims 1-3, 5, 6, 7, 9-14, 16 and 17 currently stand rejected under 35 U.S.C. §103(a) in view of United States Patent No. 4,940,951 to Sakamoto (hereinafter 'Sakamoto') and United States Patent No. 6,466,832 to Zuqert et al. (hereinafter 'Zuqert').

Based on a review of the Examiner's remarks provided in the most recent Office Action, it appears that there is some misunderstanding regarding the language of the claims. In particular, the Examiner has interpreted claim 1 to mean that a "decoder is reset and reinitialized when a transmission signal is received after a period of transmission idleness at a transmitter source" (Office action dated May 29, 2009, p. 2, section 1, para. 3) (emphasis added). The Applicant respectfully submits that the interpretation is inconsistent with the claim language. Claim 1, as presented in the previous Response, recited a processor configured to "automatically reset and reinitialize said decoder throughout a period of signal transmission idleness at a transmitter source until a transmission signal is received and a phase lock loop is established" (emphasis added). Accordingly, the claim is directed to resetting and reinitializing a decoder during ('throughout') a period of signal transmission idleness and the resetting and reinitializing is performed until a transmission signal is received and a phase lock loop is established.

Furthermore, contrary to the assertions posed in the Office Action, this interpretation of the claim language is consistent with the Specification. For example, the problem addressed by the present application is related to deficiencies in prior art systems in which long periods of transmission idleness causes a wireless receiver to cease decoding and thereby requires a user to manually re-establish a phase lock loop for decoding of audio files (see, e.g., Specification, p. 1, line 27 to p. 2, line 5). The present application addresses the problem by continually polling for a loss of a phase lock loop (PLL) at a receiver and if a decoder's phase lock loop has unlocked, the processor may repeatedly reinitialize and reset the decoder until a phase lock loop has been established (see, e.g., Specification, FIG. 3, p. 5, lines 17-24). The Specification nowhere indicates that the iterations in FIG. 3 stops and restarts when a new signal is received, as the Examiner's interpretation would indicate. Rather, FIG. 3 illustrates that from the moment the

processor detects that the PLL has unlocked, for example due to a loss of an audio file signal, the processor repetitively polls and reinitializes the decoder until a PLL is established, due, for example, to the receipt of a new signal. Thus, the decoder is polled and reinitialized repetitively during or throughout a period of transmission idleness at a transmitter.

It is respectfully submitted that claim 1 in its prior form is directed to resetting reinitializing a decoder during a period of transmission idleness until a transmission signal is received. While the Applicant believes that amendments to the claims are unnecessary, claim 1 has been amended to clarify its features. Claims 7 and 12 were amended for similar reasons.

Claim 1 recites:

> Apparatus comprising:
> a receiver for receiving an audio file signal;
> a decoder for demodulating said audio file signal; and
> a processor configured to poll said decoder for a loss of a phase lock loop in said demodulating of said audio file signal to detect audio file signal loss between the receiver and a transmitter, wherein the processor is further configured to, in response to said loss in said phase lock loop, automatically and repeatedly reset and reinitialize said decoder throughout and during a period of signal transmission idleness at a transmitter source until a transmission signal is received and a phase lock loop is established.

As noted by the Examiner, Sakamoto discloses resetting and reinitializing a PLL during data reception. However, it is respectfully submitted that Sakamoto does not disclose or render obvious repeatedly resetting and reinitializing a decoder during a period of transmission idleness at a transmitter until a transmission signal is received and a phase lock loop is established. As discussed in the response to the Office Action dated December 22, 2008, to initiate resetting and reinitiating of a PLL, Sakamoto requires that a signal be received at its apparatus. In particular, Sakamoto teaches that a frequency sweep for PLL recovery is performed in response to an error detection pulse (see, e.g., Sakamoto Column 6, lines 34-36), which is generated by analyzing PCM data extracted from a received signal (see, e.g., Sakamoto, column 6, lines 7-16). Thus, because the resetting and reinitiating of a PLL is based on a received signal, Sakamoto fails to teach that a decoder is reset and reinitialized during a period of signal transmission idleness, as recited in claim 1. Moreover, in view of Sakamoto, it would not be obvious to modify the apparatus to reset and reinitialize PLL recovery during a period of transmission idleness because there is no need to do so. During a period of transmission idleness, there is no signal onto which the PLL may lock.

Furthermore, with regard to Zuqert, Zuqert fails to cure the deficiencies of Sakamoto. While Zuqert discloses using a phase lock loop to lock on to transmission frequencies (see, e.g., Zuqert, column 18, lines 12-25), Zuqert does not disclose or render obvious responding to a loss of a phase lock loop by automatically resetting and reinitializing a decoder or a demodulator during a period of signal transmission idleness at a transmitter source. In addition, regardless of whether the transmitter in Zuqert is capable of being in an "OFF" state, as noted in the Final Office Action, the apparatus of Sakamoto requires that a signal be received to initiate resetting and reinitiating of a PLL, as discussed above. Therefore, Zuqert fails to cure the deficiencies of Sakamoto.

Accordingly, claim 1 is believed to be patentable over the cited references for at least the reasons discussed above. Likewise, claims 7 and 12 are believed to be patentable over Sakamoto and/or Zuqert, as claims 7 and 12 include similar, relevant features discussed above with respect to claim 1. Claim 7 recites, inter alia: "automatically and repetitively resetting and reinitializing said demodulating in response to said loss in said phase lock loop throughout and during a period of signal transmission idleness at a transmitter source until a transmission signal is received and a phase lock loop is established . . . ." In addition, claim 12 recites, inter alia: "automatically and repetitively resetting and reinitializing said decoding in response to said loss in said phase lock loop throughout and during a period of signal transmission idleness at a transmitter source until a transmission signal is received and a phase lock loop is established." Thus, claims 7 and 12 are believed to be patentable over Sakamoto and/or Zuqert for at least the reasons discussed above. Additionally, claims 3, 5, 6, 9-14, 16 and 17 are believed to be patentable over the cited references due at least to their dependencies from claims 1, 7 and 12. As such, withdrawal of the rejection is respectfully requested.

Claims 4, 8 and 15 stand rejected as being unpatentable over Sakamoto as modified by Zuqert in view of United States Patent No. 6,389,548, to Bowles (hereinafter 'Bowles').

Due to the dependencies of claim 4, 8 and 15 from claims 1, 7 and 12, respectively, claims 4, 8 and 15 include the feature of responding to a loss of a phase lock loop by repetitively resetting and reinitializing decoding or demodulating throughout and during a period of signal transmission idleness at a transmitter source until a transmission signal is received and a phase lock loop is established. For at least the reasons discussed above, claims 4, 8 and 15 are believed to be patentable over Sakamoto and Zuqert. Furthermore, combination of Sakamoto and/or

Zuqert with Bowles does not render claims 4, 8 and 14 obvious, as Bowles fails to cure the deficiencies of Sakamoto and/or Zuqert.

Bowles is directed to a system and method for measuring a pulse run length in a high frequency data signal (see, e.g., Bowles, Abstract). Although Bowels discloses using a phase locked loop to track changes in variations of the HF signal caused by imperfections on a compact disc, such as fingerprints (see, e.g., Bowles, column 7, lines 16-23; column 7, lines 65-67), Bowles does not disclose or render obvious responding to a loss of a phase lock loop by automatically and repetitively resetting and reinitializing decoding or a demodulating throughout and during a period of signal transmission idleness at a transmitter source until a transmission signal is received and a phase lock loop is established, as included in claims 4, 8 and 15. Thus, claims 4, 8 and 15 are believed to be patentable over Sakamoto, Zuqert and Bowles, taken singly or in any combination.

In view of the foregoing, the Applicant respectfully requests that the rejections of the claims set forth in the Office Action of May 29, 2009 be withdrawn, that pending claims 1-17 be allowed, and that the case proceed to early issuance of Letters Patent in due course.

It is believed that no additional fees or charges are currently due. However, in the event that any additional fees or charges are required at this time in connection with the application, they may be charged to the Applicant's representatives Deposit Account No. 07-0832.

Respectfully submitted,

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